REMARKS

Status of the Claims

Claims 1 and 3-30 remain pending in the present application. Applicants have cancelled Claim 2 and amended Claims 1, 3, 12, 17, 18, 21-23, 25, 27, and 30 as set forth above, to more clearly define the present invention.

Claims Rejected Under 35 U.S.C. § 102(e)

Claims 1, 2, 11-24, and 26-30 are rejected under 35 U.S.C. § 102(e) as being anticipated by Van Hook et al. (U.S. Patent No. 6,342,892, hereinafter "Van Hook"). Applicants respectfully disagree with the rejection. Nevertheless, applicants have amended independent Claims 1, 17, 23, and 30 to more clearly define the invention as further discussed below. Applicants have also amended dependent Claims 3, 12, 18, 21, 22, 25, and 27 to address corresponding antecedent basis issues that arose due to the amendments to the first set of claims. In the interest of reducing the complexity of the issues for the Examiner to consider in this response, the following discussion focuses on amended independent Claims 1, 17, 23, and 30, and the patentability of each remaining dependent claim is not necessarily separately addressed in detail. Applicants' decision not to discuss the differences between the cited art and each dependent claim should not be considered as an admission that applicants concur with the Examiner's conclusion that these dependent claims are not patentable over the disclosure in the cited references. Similarly, applicants' decision not to discuss differences between the prior art and every claim element, or every comment made by the Examiner, should not be considered as an admission that applicants concur with the Examiner's interpretation and assertions regarding those claims. Indeed, applicants believe that all of the dependent claims patentably distinguish over the references cited. However, a specific traverse of the rejection of each dependent claim is not required, since dependent claims are patentable for at least the same reasons as the independent claims from which the dependent claims ultimately depend.

With regard to independent Claim 1, applicants have incorporated the elements of original Claim 2 to clarify that the first vector functional unit obtains a vector of at least one partition of the multimedia data from the enhanced texture cache. This clarifies that applicants' first vector function unit is incorporated into a graphics rendering pipeline (as shown in FIGURE 3 of applicants' specification), and not part of a preprocessing stage of the conventional graphics coprocessor disclosed by Van Hook.

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The present Office Action refers to Figure 6 of Van Hook and indicates that a texture memory 502 is in communication with a vector unit 420 through a signal processor 400. Texture unit 502 is part of a display processor 500, whereas vector unit 420 is part of signal processor 400. Although Van Hook uses the term "vector unit," this term is not equivalent to applicants' "first vector functional unit." Van Hook's vector unit and signal processor are more closely related to applicants' host CPU 18. For example, Van Hook's Figure 3 illustrates that the signal processor performs 3D geometry transformation and lighting. However, applicants' specification defines these functions as host CPU functions in Method 2, which is shown in FIGURE 1. Applicants' specification further explains that "a preferred embodiment of the present invention focuses on extending 3D graphics pipelines in the category of Method 2, in which the graphics processor is responsible for carrying out rasterization and fragment operation layers, while the host CPU is responsible for carrying out the API and transform/lighting layers" (Specification, pg. 7, lines 18-22).

Van Hook specifies that "signal processor 400 and display processor 500 work independently . . ." (Van Hook, col. 7, lines 23-24). Van Hook further states that "the signal processor can supervise the display processor by sending graphics commands to it" (Van Hook, col. 7, lines 24-26). However, vector unit 420 never obtains commands or data from texture unit 502. In addition, Van Hook explains that "[s]ignal processor 400 also processes sound commands received from main processor 100 . . . (Van Hook, col. 8, lines 8-9). However, there is no indication that Van Hook's texture memory 502 is used for any audio data, and there is no indication that display processor 500 is involved in audio processing in any way. Thus, Van Hook does not disclose or suggest a first vector functional unit that obtains a vector of data from an enhanced texture cache, as recited in applicants' independent Claim 1. Note that a "vector of data" is not to be confused with "vector data" corresponding to graphics geometric primitives.

In providing further detail, Van Hook states that "[s]ignal processor 400 can execute instructions **only** out of instruction memory 402 . . ." (emphasis added, Van Hook, col. 15, lines 66-67). Van Hook discloses that signal processor 400 "has access to main memory 300 via direct memory accessing (DMA) techniques" (Van Hook, col. 16, lines 1-2), but there is no indication that data from texture unit 502 are ever transferred to main memory 300 for use by vector unit 420, or transferred directly to signal processor 400 via coprocessor bus 214 or private x bus 218. In fact, when discussing a DMA controller 518 of display processor 500, Van Hook states that "DMA

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controller 518 is uni-directional – that is, it can only write from [coprocessor] bus 214 into RAM 516" (Van Hook, col. 48, lines 24-25). Thus, as illustrated in Figure 20 of Van Hook, display processor 500 can use DMA controller 518 to read data from signal processor 400 via coprocessor bus 214, but not to provide data from the display processor to the signal processor. Similarly, "DMA controller 518 . . . reads data from the signal processor's data memory 404 over private 'x bus' 21[8] if the registers 518a, 518b specify a data memory 404 address." However, because DMA controller is uni-directional, it can not write data from display processor 500 to signal processor 400.

The only other avenue of communication for texture memory 502 is through a memory interface 512, which enables display processor 500 to read from and write to main memory 300 (see Van Hook, col. 56, lines 16-49). However, Van Hook explains that "[m]emory interface 512 is primarily used during normal display processor 500 operations to access the color frame buffer 118a and the Z buffer 118b" (Van Hook, col. 56, lines 18-21). Van Hook does not disclose or suggest that vector unit 420 obtains any data from color frame buffer 118a, Z buffer 118b, or any other main memory location to which memory interface 512 writes. Thus, Van Hook does not disclose or suggest that a first vector functional unit obtains a vector of at least one partition of the multimedia data from a texture cache, as recited in applicants' independent Claim 1.

Accordingly, the rejection of independent Claim 1 under 35 U.S.C. § 102(e) over Van Hook should be withdrawn. Because dependent claims are considered to include all of the elements of the independent claims from which the dependent claims ultimately depend, and because Van Hook does not disclose or suggest all of the elements of independent Claim 1, the rejection of dependent Claims 11-16 under 35 U.S.C. § 102(e) over Van Hook should also be withdrawn for at least the same reasons as the rejection of Claim 1.

With regard to independent Claim 17, applicants have carried over the idea that the programmable graphics pipeline comprises a programmable graphics rendering pipeline by clarifying that the programmable graphics pipeline performs graphics rendering processing on graphics texture data to produce pixel output data when a partitioned data size and instruction correspond to graphics processing, yet the same programmable graphics rendering pipeline performs media processing on media source data when the partitioned data size and the instruction correspond to media processing. Note that the graphics rendering processing also includes processing corresponding coordinate data, along with graphics texture data, as defined in dependent Claims 18-20.

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Support for this rendering aspect is found at numerous locations in the specification, including page 16, lines 5-6, which state that "[w]hile the additional computing power of VPE 60 enables multimedia processing, the architecture does not slow the rendering throughput for 3D graphics." The specification further explains that:

> Producing graphics pixel data is done in a well-known manner by mapping texture data from perspective inverse-mapped coordinates to output pixel coordinates, preferably using bilinear or trilinear filtering of 32-bit graphics data. By comparison, producing image pixel data employs the mapping technique with partitioned data, preferably 8-bit or 16-bit data. In a manner similar to the graphics processing, the programmable graphics pipeline is used to produce output coordinates, to produce mapped image coordinates corresponding to the output coordinates, and to produce memory addresses, where image data are stored corresponding to the mapped image coordinates. However, instead of retrieving texture data, the programmable graphics pipeline retrieves image data from the memory addresses and stores the retrieved data in the enhanced texture cache. The programmable pipeline then executes instructions corresponding to the desired image manipulation function on the retrieved data to produce the image pixel data at the output coordinate. (Specification, pg. 4, lines 21-33.)

In general, "the programmable graphics pipeline is capable of producing any form of corresponding multimedia output data, such as audio data, graphics pixel data, image pixel data, video pixel data, etc., depending on processing instructions and data access parameters identified by a host processor" (Specification, pg. 2, lines 35-38). Amended Claim 17 clarifies that the same programmable graphics rendering pipeline can perform both functions of rendering graphics texture data to produce graphics pixel data and processing media source data (including both audio data and visual data) to produce media output data, which is, by definition, different from the media source data, as a result of the processing.

The Office Action indicates that Van Hook "shows in Fig. 7B an example slicing of the instruction format for processing by the vector unit" (Office Action, pg. 3, lines 12-13). The Office Action further refers to Figure 3 as showing that Van Hook's signal processor "not only performs graphics commands, but also sound (media) commands," and that "data after being processed is stored in main memory 128 and 132" (Office Action, pg. 3, lines 14-15). However, Van Hook does not disclose or suggest performing graphics rendering processing and media processing with the same

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programmable graphics rendering pipeline. Instead, Figure 3 of the cited art shows that Van Hook uses the signal processor to perform initial geometry transformation and lighting and to perform audio processing. Van Hook's signal processor does not perform graphics rendering processing on graphics texture data. For graphics rendering processing, Van Hook requires the display processor to apply texture data to the transformed geometry produced by the signal processor. Because Van Hook uses the display processor to perform graphics rendering processing, but uses the signal processor to perform media (audio) processing, Van Hook does not disclose or suggest applicants' claimed steps of performing graphics rendering processing and media processing with the same programmable graphics rendering pipeline. Accordingly, the rejection of independent Claim 17 under 35 U.S.C. § 102(e) over Van Hook should be withdrawn. Because dependent claims are considered to include all of the elements of the independent claims from which the dependent claims depend, and Van Hook does not disclose or suggest all of the elements of independent Claim 17, the rejection of dependent Claims 18-22 under 35 U.S.C. § 102(e) over Van Hook should also be withdrawn for at least these same reasons.

With regard to amended independent Claim 23, applicants have again clarified the rendering scope and the distinction between graphics processing and media processing by indicating that source variable length data can comprise graphic texture source data or media source data, yet both are processed by the same vector processing engine (VPE) that generates graphics pixel data or media pixel data, respectively. Support for the amendment to this claim is found at the locations of the specification cited above. The Office Action does not separately address the elements of independent Claim 23, but instead relies on those portions of Van Hook cited against independent Claim 1. Applicants thus rely on the discussion above that distinguishes applicants' claimed invention over the cited portions of Van Hook. In addition, applicants note that the specification of the present application defines the VPE as comprising the "vector functional unit (VFU) 62, an instruction cache 64, and a register file 66" (Specification, pg. 15, lines 20-21). These components correspond to the recited elements of independent Claim 1, but an enhanced texture cache need not be added to independent Claim 23, because independent Claim 23 already includes a memory from which the graphics texture source data and the media source data are accessed. Accordingly, the rejection of independent Claim 23 under 35 U.S.C. § 102(e) over Van Hook should be withdrawn. Because dependent claims are considered to include all of the elements of the independent claims from which

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the dependent claims depend, and Van Hook does not disclose or suggest all of the elements of independent Claim 23, the rejection of dependent Claims 24, and 26-29 under 35 U.S.C. § 102(e) over Van Hook should also be withdrawn for at least these reasons.

With regard to amended independent Claim 30, applicants have again clarified that variable length data can comprise graphic **texture** data or media source data, yet both are processed by the same vector processing engine (VPE). Support is found in the specification at the locations cited above. The amendment to Claim 30 clarifies that Van Hook's vector unit 420 cannot be interpreted as applicants' VPE, because Van Hook does not disclose or suggest that graphics texture data are cached in data memory 404. Further, as discussed above, Van Hook does not disclose or suggest that vector unit 420 can access graphics texture data or be used to perform a graphics function on graphics texture data. Instead, as illustrated in Van Hook's Figure 3, vector unit 420 is limited to geometry transformation and lighting, thereby requiring a separate display processor 500 to operate on graphics texture data. Accordingly, the rejection of independent Claim 30 under 35 U.S.C. § 102(e) over Van Hook should be withdrawn.

Claims Rejected Under 35 U.S.C. § 103(a)

Claims 3-10 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Van Hook in view of Gossett (U.S. Patent No. 6,104,415). However, Claims 3-10 and 25 depend from independent Claims 1 and 23, which are patentable for the reasons discussed above. The Office Action does not indicate that Gossett discloses or suggests the claim elements that Van Hook fails to disclose or suggest. Thus, the combination of Van Hook and Gossett still does not disclose or suggest all of the elements of applicants' independent Claims 1 and 23. Because dependent claims are considered to include all of the elements of the independent claims from which the dependent claims depend, dependent Claims 3-10 and 25 are patentable for at least the same reasons discussed above with regard to independent Claims 1 and 23. Accordingly, the rejection of dependent Claims 3-10 and 25 under 35 U.S.C. § 103(a) over Van Hook in view of Gossett should be withdrawn.

Further, with regard to Claim 3, the Office Action indicates that Gossett teaches a texture cache 74 comprising a table 75 and a memory 87. The Office Action states that "Table 75 stores a mapped relationship between the texel numbers indicated by the texel address 72 to the SDRAM addresses (line buffer)" (Office Action, pg. 5, lines 4-5). It is unclear which element of Gossett that the Examiner considers to disclose or suggest applicants' line buffer. Figure 4 of Gossett illustrates that the

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SDRAM is separate from texture unit 58, which includes texture cache 74, as shown in Figure 10. Thus, applicants infer that the Examiner does not interpret the SDRAM disclose or suggest applicants' line buffer. Consequently, applicants must presume that the Examiner considers Gossett's table 75 to disclose or suggest applicants' line buffer. However, Gossett's table 75 does not disclose or suggest multiple read ports as required by Claim 3. Instead, Gossett explains that "table 75 stores the starting address of the texture [in SDRAM], along with the stride value . . ." (Gossett, col. 16, lines 60-61). The stride value indicates a number of texel values to skip (in both the s and t directions) when retrieving texel values from the SDRAM for storage in memory 87 of texture cache 74 (see, Gossett, col. 16, lines 17-18 and 35-50). Storing a starting address and stride value does not suggest multiple read ports. Thus, table 75 does not disclose or suggest applicants' line buffer, which is a recited element of Claim 3. Accordingly, the rejection of at least dependent Claim 3 under 35 U.S.C. § 103(a) over Van Hook in view of Gossett should be withdrawn. Further, Claims 4-9 ultimately depend from Claim 3. Because dependent claims are considered to include all of the elements of the intervening claims from which the dependent claims depend, dependent Claims 4-9 are patentable for at least the same reasons discussed above, with regard to Claim 3. Accordingly, the rejection of at least dependent Claims 4-9 under 35 U.S.C. § 103(a) over Van Hook in view of Gossett should also be withdrawn.

In consideration of the amendment to the application and the Remarks set forth above, it is submitted that all claims in the application define a novel and non-obvious invention and are thus patentable. The Examiner is therefore requested to pass this case to issue without delay. Should any further questions remain, the Examiner is invited to telephone applicants' attorney at the number listed below.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 30, 2004.

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